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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/720,133	11/25/2003	Takashi Fujiwara	245818US2	4411

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EXAMINER	
SIKRI, ANISH	
ART UNIT	**PAPER NUMBER**
2143	

NOTIFICATION DATE	DELIVERY MODE
02/21/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/720,133	FUJIWARA, TAKASHI	
	Examiner	Art Unit	
	ANISH SIKRI	2143	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 December 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 11-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 11-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/25/03, 04/13/06, 09/22/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

The information disclosure statement submitted on 11/25/03, 04/13/06, 9/22/06 been considered by the Examiner and made of record in the application file.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-6, are rejected under 35 U.S.C. 103(a) as being unpatentable by Zulian et al (US Patent 5,701,413), in view of Waldecker et al (US Pat 4,669,056).

Claims 7-8, 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zulian et al (US Patent 5,701,413), in view of Waldecker et al (US Pat 4,669,056), and in further view of Cohen (US Patent 6,026,464).

Consider **Claim 1**, Zulian et al clearly discloses a data transfer system comprising: a plurality of requesters (Zulian et al, Col 4, Lines 16-24), configured to send data transfer requests (Zulian et al, Col 4, Lines 25-27), the requesters configured to transfer data when authorized (Zulian et al, Col 4, Lines 29-35); a transfer controller configured to receive the data transfer requests from the requesters (Zulian et al, Col 4, Lines 29-35, Lines 36-42), the transfer controller configured to authorize one of the data transfer requests to perform arbitration for the data transfer requests (Zulian et al, Col 4, Lines 29-35, Lines 36-42), the transfer controller configured to send a transfer directive at a predetermined timing (Zulian et al, Col 4, Lines 43-48, Lines 53-58); a network configured to receive the transfer directive to transfer data from an authorized requester based on the transfer directive (Zulian et al, Col 4, Lines 43-48, Lines 53-58); and a plurality of memories including a plurality of modules (Zulian et al, Col 4, Lines 16-24), each of the modules having data input and output unit (Zulian et al, Col 4, Lines 16-24,

Lines 43-48), the memories configured to receive the transfer directive to receive transfer data from the network based on the transfer directive (Zulian et al, Col 4, Lines 16-24, Lines 43-48), wherein the transfer controller comprises: a request storing unit configured to receive data transfer requests from the requesters (Zulian et al, Col 4, Lines 29-58),

But Zulian fails to disclose an address decoder configured to decode addresses of the data transfer requests stored in the request storing unit; a module arbitration unit configured to perform arbitrations of decoded data transfer requests on a per-module basis, the module arbitration unit including a plurality of module arbiters that hold the decoded data transfer requests for each module; a network arbitration unit configured to perform arbitrations of the decoded data transfer requests for allocating the network; and a transfer directive generator configured to generate transfer directives related to data transfers requests that are granted authorization to use the network by module arbitration unit and network arbitration unit.

Nonetheless, Waldecker et al discloses an address decoder configured to decode addresses of the data transfer requests stored in the request storing unit (Waldecker et al, Col 2 Lines 51-69, Col 1-10, Col 4 Lines 8-27); a module arbitration unit configured to perform arbitrations of decoded data transfer requests on a per-module basis (Waldecker et al, Col 2, Lines 57-61), the module arbitration unit including a plurality of module arbiters that hold the decoded data transfer requests for each module (Waldecker et al, Col 2 Lines 57-61, Col 4 Lines 45-51); a network arbitration unit configured to perform arbitrations of the decoded data transfer requests for

allocating the network (Waldecker et al, Col 2 Lines 50-52); and a transfer directive generator configured to generate transfer directives related to data transfers requests that are granted authorization to use the network by module arbitration unit and network arbitration unit (Waldecker et al, Col 2 Lines 47-52, Col 4 Lines 30-43).

Therefore, it would have been obvious to person skilled in the art to incorporate the use of a networked unit/controller which is capable of arbitration of decoded data along with its addresses which are being into the storing unit (memory, buffers etc) for processing and transferring (with its transfer directives) to the network, taught by Waldecker et al in the system of Zulian et al for the purpose of reducing or eliminating the use of a intermediate buffer between memories (storage) and transfer controller as data is processed in the memory itself, thus increasing performance.

Consider **Claim 2**, Zulian et al, in view of Waldecker et al, clearly discloses the data transfer system of claim 1, wherein the transfer controller performs arbitration for the memories then performs arbitration for the network (Zulian et al, Col 4, Lines 43-48, Lines 53-58). Zulian et al clearly shows on how the timing commands and received from the memories and the processors of the system.

Consider **Claim 3**, Zulian et al, in view of Waldecker et al, clearly discloses the data transfer system of claim 1, wherein the data transfer controller performs arbitration for the network then performs arbitration for the memories (Zulian et al, Col 4, Lines 16-

24, Lines 43-48, Lines 53-58). Zulian et al clearly shows on how the timing commands and received from the memories of the system.

Consider **Claim 4**, Zulian et al, in view of Waldecker et al, clearly discloses the data transfer system as claimed in claim 1, wherein the transfer controller performs arbitration for the network and arbitration for the memories in parallel (Zulian et al, Col 4, Lines 16-24, Lines 53-58, Lines 59-61). Zulian et al clearly shows on how one control unit generates a timing signal of a predetermined frequency, which is used for controlling system memory and network processors of the system in parallel.

Consider **Claim 5**, Zulian et al, in view of Waldecker et al, clearly discloses the data transfer system as claimed in claim 1, wherein a data width of the network and data input and output width of the memories are equal (Zulian et al, Col 4, Lines 59-61). Zulian et al clearly shows that the data width of the network data and data input and output width are equal as it holds only one unit of data, which is used for the read/write operations.

Consider **Claim 6**, Zulian et al, in view of Waldecker et al, clearly discloses the data transfer system as claimed in claim 1, wherein the transfer controller detects that the data transfer requests from the requesters are read access or write access, then the transfer controller controls the timing to send transfer directives based on the access

(Zulian et al, Col 4, Lines 59-61, Col 5, Lines 49-61). Zulian et al clearly shows on how the data transfer system with the aid of timing unit conducts its read or write access.

Consider **Claim 7**, Zulian et al, in view of Waldecker et al, fails to disclose wherein the plurality of modules includes a plurality of macros, the data is divided to be stored by the plurality of macros.

Nonetheless, Cohen teaches data transfer system as claimed in claim 1, wherein the plurality of modules includes a plurality of macros, the data is divided to be stored by the plurality of macros (Col 1, Lines 53-60, Col 3 Lines 13-15).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the use of plurality of macros (memory) having the ability to store divided data taught by Cohen, in the system of Zulian et al, as modified by Waldecker et al, for the purpose of enabling robust communication between the network system and its processors and memory (Cohen, Col 1, Lines 20-21).

Consider **Claim 8**, Zulian et al, in view of Waldecker et al, fails to disclose the data transfer system as claimed in claim 1, wherein the transfer controller controls transferring the data based on a major cycle defined to be at least two clock cycles.

Nonetheless, Cohen teaches the data transfer system as claimed in claim 1, wherein the transfer controller controls transferring the data based on a major cycle defined to be at least two clock cycles (Cohen, Col 4 Lines 5-12, 59-61).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the use transfer controller using cycle based timing to transfer data taught by Cohen, in the system of Zulian et al, as modified by Waldecker et al for the purpose of data transfer timing mechanism to ensure timed and controlled robust communication in the system.

Consider **Claim 11**, Zulian et al, as modified by Waldecker et al, fails to disclose the data transfer system as claimed in claim 1, wherein each of the module arbiters selects a macro that can currently be accessed earliest among the data transfer requests.

Nonetheless, Cohen clearly discloses the data transfer system as claimed in claim 1, wherein each of the module arbiters selects a macro that can currently be accessed earliest among the data transfer requests (Cohen, Col 5, Lines 24-30).

Therefore, it would have been obvious to incorporate the use of module arbiters selecting macros (data first in-first out buffer/memory), taught by Cohen, to be integrated with the system of Zulian et al, as modified by Waldecker et al, for the selection of macro/memory which obtains the earliest data when it is being transferred in the system.

Consider **Claim 12**, Zulian et al, as modified by Waldecker et al, fails to disclose the data transfer system as claimed in claim 1, wherein each of the module arbiters selects a data transfer request requesting to an accessible macro based on the response time of the macro.

Nonetheless, Cohen clearly discloses the data transfer system as claimed in claim 1, wherein each of the module arbiters selects a data transfer request requesting to an accessible macro based on the response time of the macro (Cohen, Col 5, Lines 24-30, Col 6, Lines 8-14, 35-47).

Therefore, it would have been obvious to incorporate the use of module arbiters selecting macros, taught by Cohen, in the system of Zulian et al, as modified by Waldecker et al, for the request of requesting data stored in the macro/memory of the system.

Consider **Claim 13**, Zulian et al, as modified by Waldecker et al, fails to disclose the data transfer system as claimed in claim 1, wherein each of the module arbiters receives priority information for transferring of the requesters to select a request having the highest priority among the data transfer requests.

Nonetheless, Cohen clearly discloses the data transfer system as claimed in claim 1, wherein each of the module arbiters receives priority information for transferring of the requesters to select a request having the highest priority among the data transfer requests (Cohen, Col 6, Lines 35-47).

Therefore, it would have been obvious to incorporate the use of module arbiters receiving priority data, taught by Cohen, in the system of Zulian et al, as modified by Waldecker et al, for the request of selecting highest priority data for transfer in the system, and thus increasing the efficiency in the system.

Consider **Claim 14**, Zulian et al, as modified by Waldecker et al fails to disclose the data transfer system as claimed in claim 1, wherein the network arbitration unit allocates, per a major cycle defined to be at least two clock cycles, a network

connection of the network to requesters in consideration of read and write cycles based on the number of the buses of the network.

Nonetheless, Cohen teaches the data transfer system as claimed in claim 1, wherein the network arbitration unit allocates, per a major cycle defined to be at least two clock cycles, a network connection of the network to requesters in consideration of read and write cycles based on the number of the buses of the network (Cohen, Col 4 Lines 5-12, 59-61).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the use transfer controller using cycle based timing to transfer data taught by Cohen, in the system of Zulian et al, as modified by Waldecker et al for the purpose of data transfer timing mechanism to ensure timed and controlled robust communication in the system.

Response to Arguments

Applicant's arguments filed 12/13/2007 have been fully considered but they are not persuasive.

Applicant argues that Zulian et al does not disclose the concept of transfer directives or their use of their functionality (as the transfer controller controls the data transfer timing for the memories, in the system). Zulian et al discloses as the transfer controller controls the data transfer timing for the memories in the system (Zulian et al, Col 4, Lines 43-48, Lines 53-58). Zulian shows that the unit transfers data to memory on basis of timing commands received from the unit between the processors of the unit (Zulian et al, Col 4 Lines 37-58). And the operation of the system is clocked and synchronized by receiving periodic signal in the system, which aids the transfer controller in transferring data (Zulian et al, Col 4 Lines 65-67).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ANISH SIKRI whose telephone number is 5712701783. The examiner can normally be reached on 8am - 5pm Monday - Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Anish Sikri
a.s.

February, 10 2008

NATHAN FLYNN
SUPERVISORY PATENT EXAMINER